

TMS27C128 131 072-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY

TMS27PC128 131 072-BIT PROGRAMMABLE READ-ONLY MEMORY

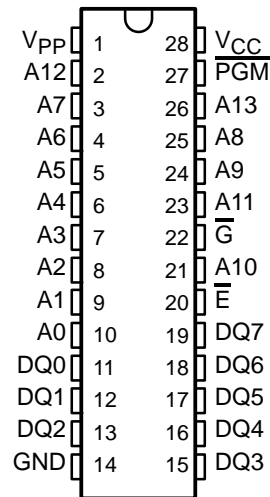
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This Data Sheet is Applicable to All TMS27C128s and TMS27PC128s Symbolized with Code "B" as Described on Page 12.

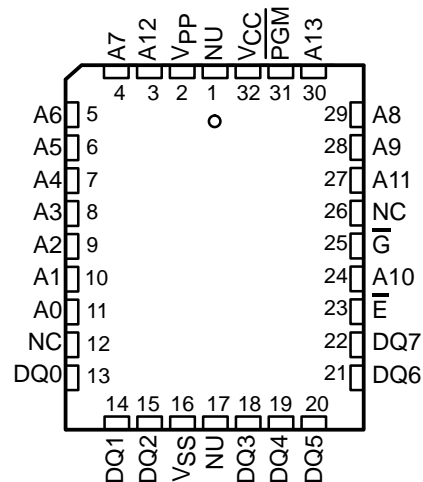
- **Organization . . . 16K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 128K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**
V_{CC} ± 10%

| | |
|---------------|--------|
| '27C128-12 | 120 ns |
| '27C/PC128-15 | 150 ns |
| '27C/PC128-20 | 200 ns |
| '27C/PC128-25 | 250 ns |
- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
 - Active . . . 158 mW Worst Case
 - Standby . . . 1.4 mW Worst Case (CMOS Input Levels)
- **PEP4 Version Available With 168-Hour Burn-In and Choices of Operating Temperature Ranges**
- **128K EPROM Available With MIL-STD-883C Class B High-Reliability Processing (SMJ27C128)**

**J AND N PACKAGES
(TOP VIEW)**



**FM PACKAGE
(TOP VIEW)**



description

The TMS27C128 series are 131 072-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC128 series are 131 072-bit, one time electrically programmable read-only memories.

PIN NOMENCLATURE

| | |
|-----------------|----------------------------------|
| A0–A13 | Address Inputs |
| \overline{E} | Chip Enable/Powerdown |
| G | Output Enable |
| GND | Ground |
| NC | No Connection |
| NU | Make No External Connection |
| PGM | Program |
| DQ0–DQ7 | Inputs (programming)/Outputs |
| V _{CC} | 5-V Power Supply |
| V _{PP} | 12-13 V Programming Power Supply |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C128 and the TMS27PC128 are pin compatible with 28-pin 128K MOS ROMs, PROMs, and EPROMs.

The TMS27C128 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C128 is offered with two operating temperature ranges of 0°C to 70°C (JL suffix) and -40°C to 85°C (JE suffix). The TMS27C128 is also offered with 168-hour burn-in temperature ranges (JL4 and JE4 suffixes). (See table below).

The TMS27PC128 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC128 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC128 is also offered with two operating temperature ranges of 0°C to 70°C (NL and FML suffixes) and -40°C to 85°C (NE and FME suffixes). The TMS27PC128 is also offered with 168 hour burn-in temperature ranges (NL4, FML4, NE4, and FME4 suffixes). (See table below).

All package styles conform to JEDEC standards.

| EPROM AND PROM | SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN | | SUFFIX FOR OPERATING TEMPERATURE RANGES WITH PEP4 168 HR. BURN-IN | |
|----------------------|--|----------------|---|----------------|
| | 0°C TO 70°C | -40 °C TO 85°C | 0°C TO 70°C | -40 °C TO 85°C |
| TMS27C128-XXX | JL | JE | JL4 | JE4 |
| TMS27PC128-XXX | NL | NE | NL4 | NE4 |
| TMS27PC128-XXX | FML | FME | FML4 | FME4 |

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable by using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of two seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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operation

The seven modes of operation are listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

| FUNCTION | MODE | | | | | | | |
|------------------|----------|-------------------|-------------|-------------|----------|--------------------|---------------------|--------|
| | READ | OUTPUT DISABLE | STANDBY | PROGRAMMING | VERIFY | PROGRAM INHIBIT | SIGNATURE MODE | |
| \overline{E} | V_{IL} | V_{IL} | V_{IH} | V_{IL} | V_{IL} | V_{IH} | V_{IL} | |
| \overline{G} | V_{IL} | V_{IH} | X^\dagger | V_{IH} | V_{IL} | X | V_{IL} | |
| \overline{PGM} | V_{IH} | V_{IH} | X | V_{IL} | V_{IH} | X | V_{IH} | |
| V_{PP} | V_{CC} | V_{CC} | V_{CC} | V_{PP} | V_{PP} | V_{PP} | V_{CC} | |
| V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | |
| A9 | X | X | X | X | X | X | V_H V_H^\dagger | |
| A0 | X | X | X | X | X | X | V_{IL} V_{IH} | |
| DQ0–DQ7 | Data Out | HI-Z | HI-Z | Data In | Data Out | HI-Z | CODE | |
| | | | | | | | MFG | DEVICE |
| | | | | | | | 97 | 83 |

† X can be V_{IL} or V_{IH} .
 $V_H = 12\text{ V} \pm 0.5\text{ V}$.

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read/output disable

When the outputs of two or more TMS27C128s or TMS27PC128s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the \overline{E} and \overline{G} pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS27C128 and TMS27PC128 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μ A (TTL-level inputs) or 250 μ A (CMOS-level inputs) by applying a high TTL or CMOS signal to the \overline{E} pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C128)

Before programming, the TMS27C128 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are at the logic high level. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity \times exposure time) is 15-W-s/cm². A typical 12-mW/cm², filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C128, the window should be covered with an opaque label.

initializing (TMS27PC128)

The one-time programmable TMS27PC128 PROM is provided with all bits at the logic high level. The logic lows are programmed into the desired locations. Logic lows programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 128K EPROM and PROM are programmed using the TI SNAP! Pulse programming algorithm, illustrated by the flowchart in Figure 1, which programs in a nominal time of two seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, \overline{PGM} is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μ s) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100- μ s pulses per byte are provided before a failure is recognized.

The programming mode is achieved when $V_{PP} = 13$ V, $V_{CC} = 6.5$ V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5$ V.

program inhibit

Programming may be inhibited by maintaining a high level input on the \overline{E} or \overline{PGM} pin.

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program verify

Programmed bits may be verified with $V_{PP} = 13 \text{ V}$ when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to $12 \text{ V} \pm 0.5 \text{ V}$. Two identifier bytes are accessed by A0; i.e., $A0 = V_{IL}$ accesses the manufacturer code, which is output on DQ0–DQ7; $A0 = V_{IH}$ accesses the device code, which is output on DQ0–DQ7. All other addresses must be held at V_{IL} . The manufacturer code for these devices is 97, and the device code is 83.



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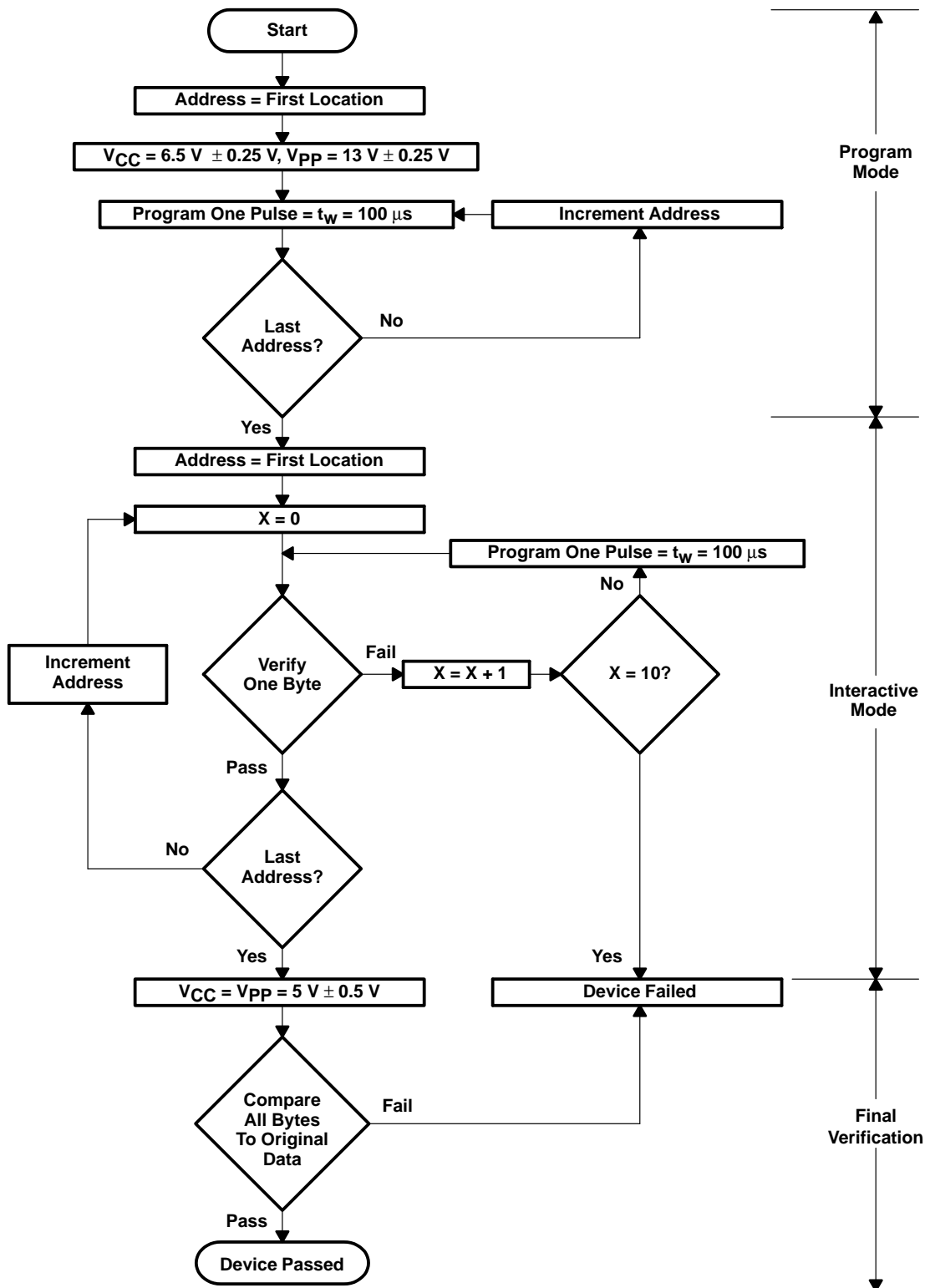
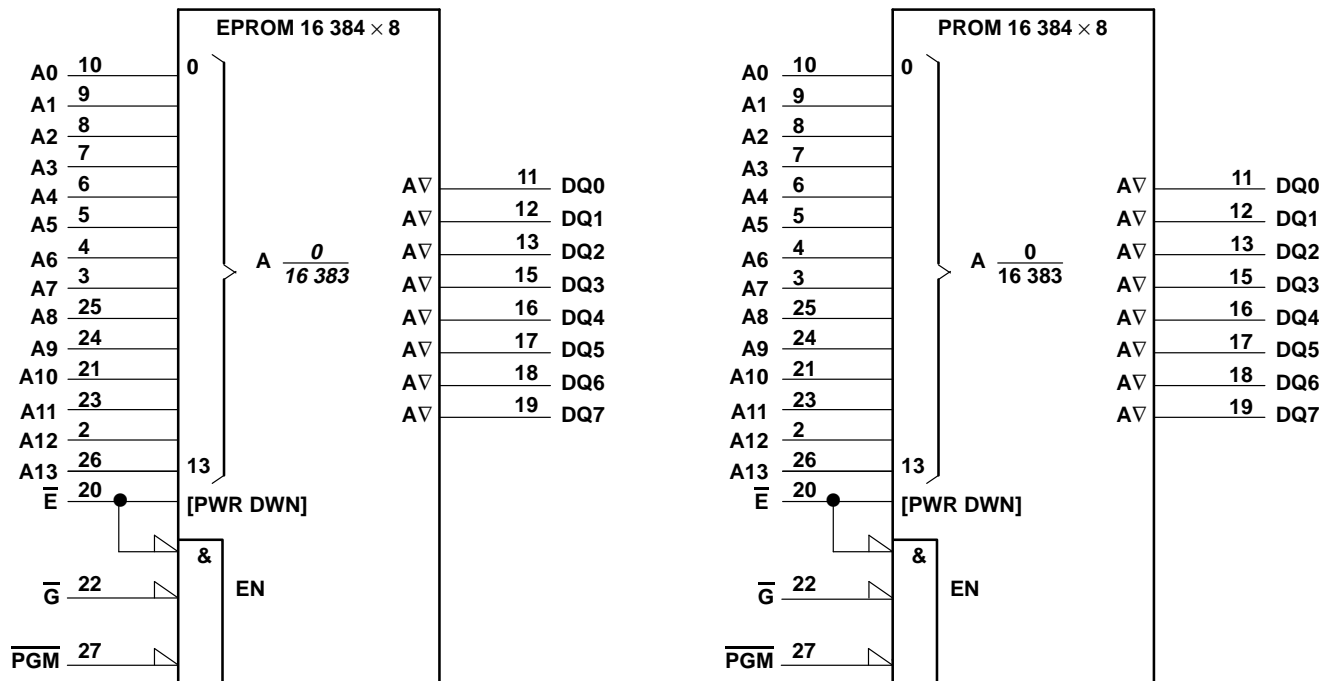


Figure 1. SNAP! Pulse Programming Flowchart

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logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|--------------------------|
| Supply voltage range, V_{CC} (see Note 1) | −0.6 V to 7 V |
| Supply voltage range, V_{PP} (see Note 1) | −0.6 V to 14 V |
| Input voltage range (see Note 1), All inputs except A9 | −0.6 V to $V_{CC} + 1$ V |
| A9 | −0.6 V to 13.5 V |
| Output voltage range (see Note 1) | −0.6 V to $V_{CC} + 1$ V |
| Operating free-air temperature range ('27C128-__JL and JL4, '27PC128-__NL, and NL4 FML, and FML4) | 0°C to 70°C |
| Operating free-air temperature range ('27C128-__JE and JE4, '27PC128-__NE, NE4, FME, and FME4) | −40°C to 85°C |
| Storage temperature range | −65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.



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recommended operating conditions

| | | MIN | NOM | MAX | UNIT | |
|-----------------|--------------------------------|-----------------------------------|-----------------------|-----|-----------------------|---|
| V _{CC} | Supply voltage | Read mode (see Note 2) | 4.5 | 5 | 5.5 | V |
| | | SNAP! Pulse programming algorithm | 6.25 | 6.5 | 6.75 | |
| V _{PP} | Supply voltage | Read mode | V _{CC} - 0.6 | | V _{CC} + 0.6 | V |
| | | SNAP! Pulse programming algorithm | 12.75 | 13 | 13.25 | |
| V _{IH} | High-level dc input voltage | TTL | 2 | | V _{CC} + 1 | V |
| | | CMOS | V _{CC} - 0.2 | | V _{CC} + 1 | |
| V _{IL} | Low-level dc input voltage | TTL | -0.5 | | 0.8 | V |
| | | CMOS | -0.5 | | 0.2 | V |
| T _A | Operating free-air temperature | | 0 | 70 | °C | |
| T _A | Operating free-air temperature | | -40 | 70 | °C | |

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|---|--|--|------|-----|------|
| V _{OH} | High-level dc output voltage | I _{OH} = -2.5 mA | 3.5 | | | V |
| | | I _{OH} = -20 μA | V _{CC} - 0.1 | | | V |
| V _{OL} | Low-level dc output voltage | I _{OL} = 2.1 mA | | | 0.4 | V |
| | | I _{OL} = 20 μA | | | 0.1 | V |
| I _I | Input current (leakage) | V _I = 0 to 5.5 V | | | ±1 | μA |
| I _O | Output current (leakage) | V _O = 0 to V _{CC} | | | ±1 | μA |
| I _{PP1} | V _{PP} supply current | V _{PP} = V _{CC} = 5.5 V | | 1 | 10 | μA |
| I _{PP2} | V _{PP} supply current (during program pulse) | V _{PP} = 13 V | | 35 | 50 | mA |
| I _{CC1} | V _{CC} supply current (standby) | TTL-input level | V _{CC} = 5.5 V, \bar{E} = V _{IH} | 250 | 500 | μA |
| | | CMOS-input level | V _{CC} = 5.5 V, \bar{E} = V _{CC} | 100 | 250 | μA |
| I _{CC2} | V _{CC} supply current (active) | V _{CC} = 5.5 V, \bar{E} = V _{IL} , t _{cycle} = minimum cycle time, outputs open | | 15 | 30 | mA |

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------|--------------------|-----|------|-----|------|
| C _i | Input capacitance | | 6 | 10 | pF |
| C _O | Output capacitance | | 10 | 14 | pF |

† Typical values are at T_A = 25°C and nominal voltages.
Capacitance measurements are made on sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

| PARAMETER | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C128-12 | | '27C/PC128-15 | | UNIT | |
|---|---|------------|-----|---------------|-----|------|----|
| | | MIN | MAX | MIN | MAX | | |
| $t_{a(A)}$ Access time from address | $C_L = 100$ pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | | 120 | | 150 | ns | |
| $t_{a(E)}$ Access time from chip enable | | | 120 | | 150 | ns | |
| $t_{en(G)}$ Output enable time from \overline{G} | | | 55 | | 75 | ns | |
| t_{dis} Output disable time from \overline{G} or \overline{E} , whichever occurs first† | | | 0 | 45 | 0 | 60 | ns |
| $t_{v(A)}$ Output data valid time after change of address, \overline{E} , or \overline{G} , whichever occurs first† | | | 0 | | 0 | | ns |

| PARAMETER | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C/PC128-20 | | '27C/PC128-25 | | UNIT | |
|---|---|---------------|-----|---------------|-----|------|----|
| | | MIN | MAX | MIN | MAX | | |
| $t_{a(A)}$ Access time from address | $C_L = 100$ pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | | 200 | | 250 | ns | |
| $t_{a(E)}$ Access time from chip enable | | | 200 | | 250 | ns | |
| $t_{en(G)}$ Output enable time from \overline{G} | | | 75 | | 100 | ns | |
| t_{dis} Output disable time from \overline{G} or \overline{E} , whichever occurs first† | | | 0 | 60 | 0 | 60 | ns |
| $t_{v(A)}$ Output data valid time after change of address, \overline{E} , or \overline{G} , whichever occurs first† | | | 0 | | 0 | | ns |

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: $V_{CC} = 6.5$ V and $V_{PP} = 13$ V (SNAP! Pulse), $T_A = 25^\circ\text{C}$ (see Note 3)

| PARAMETER | MIN | NOM | MAX | UNIT |
|--|-----|-----|-----|------|
| $t_{dis(G)}$ Output disable time from \overline{G} | 0 | | 130 | ns |
| $t_{en(G)}$ Output enable time from \overline{G} | | | 150 | ns |

recommended timing requirements for programming: $V_{CC} = 6.5$ V and $V_{PP} = 13$ V (SNAP! Pulse), $T_A = 25^\circ\text{C}$ (see Note 3)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|-----------------------------------|-----|-----|-----|---------------|
| $t_w(\text{IPGM})$ Initial program pulse duration | SNAP! Pulse programming algorithm | 95 | 100 | 105 | μs |
| $t_{su(A)}$ Address setup time | | 2 | | | μs |
| $t_{su(E)}$ \overline{E} setup time | | 2 | | | μs |
| $t_{su(G)}$ \overline{G} setup time | | 2 | | | μs |
| $t_{su(D)}$ Data setup time | | 2 | | | μs |
| $t_{su(VPP)}$ V_{PP} setup time | | 2 | | | μs |
| $t_{su(VCC)}$ V_{CC} setup time | | 2 | | | μs |
| $t_h(A)$ Address hold time | | 0 | | | μs |
| $t_h(D)$ Data hold time | | 2 | | | μs |

- NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference page 10).
 4. Common test conditions apply for t_{dis} except during programming.

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PARAMETER MEASUREMENT INFORMATION

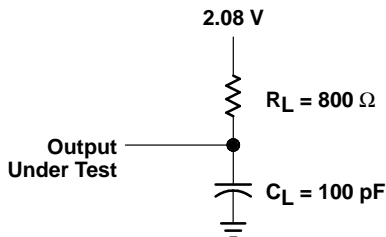
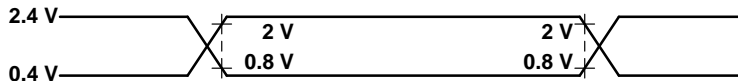


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

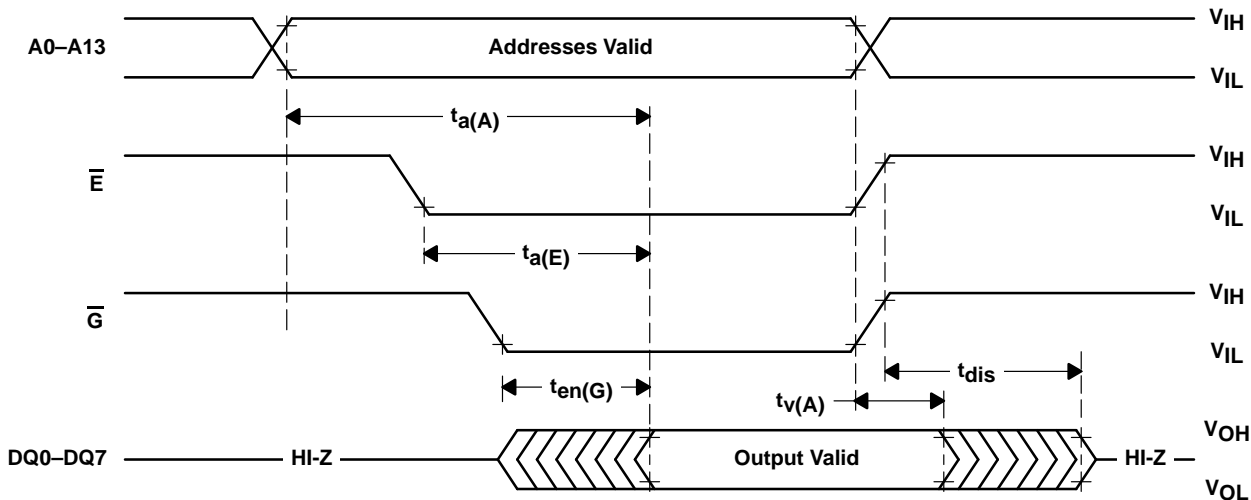
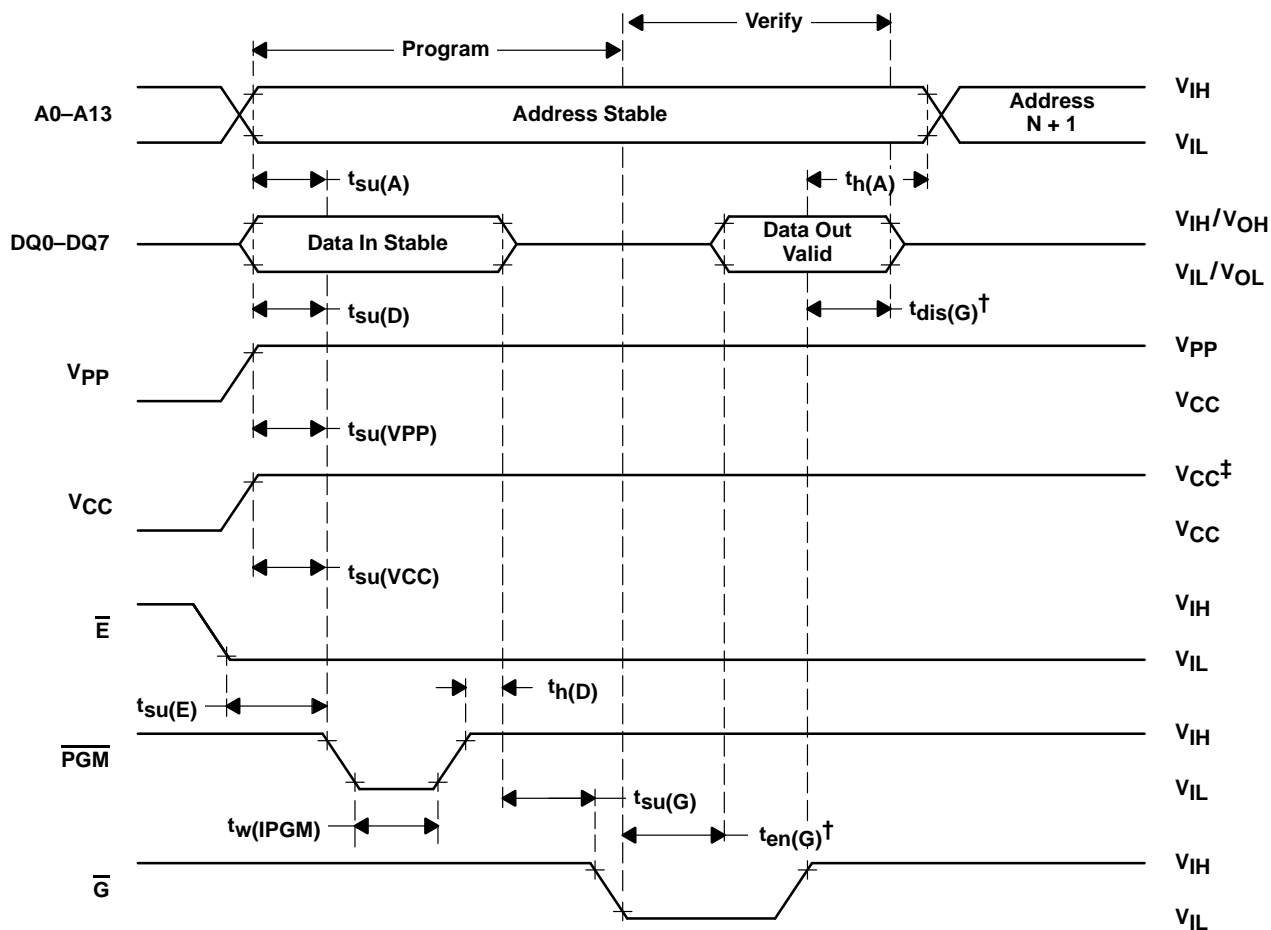


Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



[†] $t_{dis}(G)$ and $t_{en}(G)$ are characteristics of the device but must be accommodated by the programmer.
 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

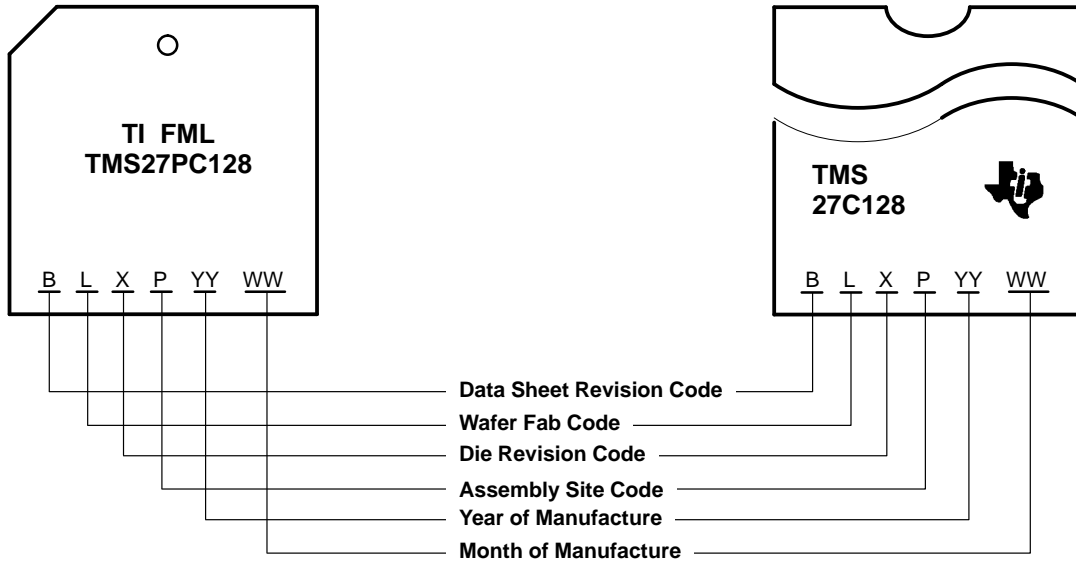
Figure 4. Program Cycle Timing

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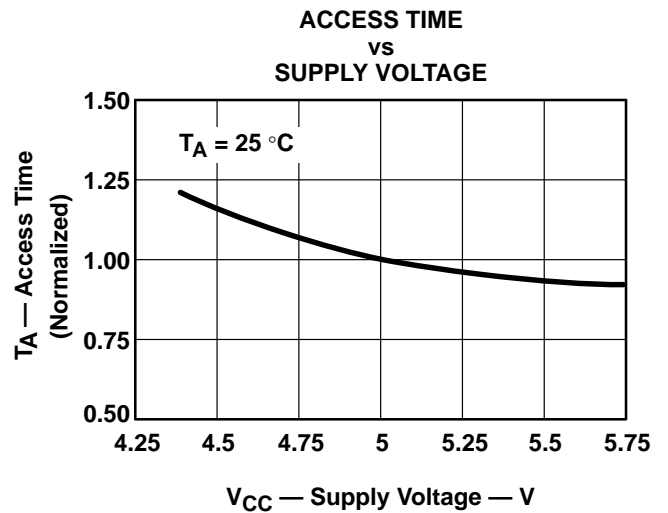
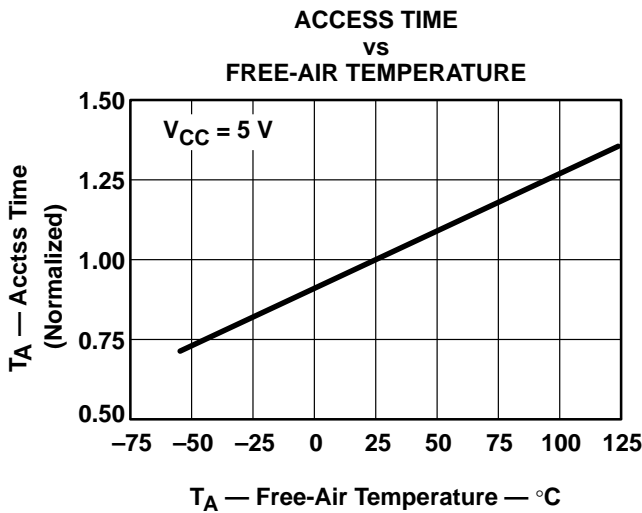
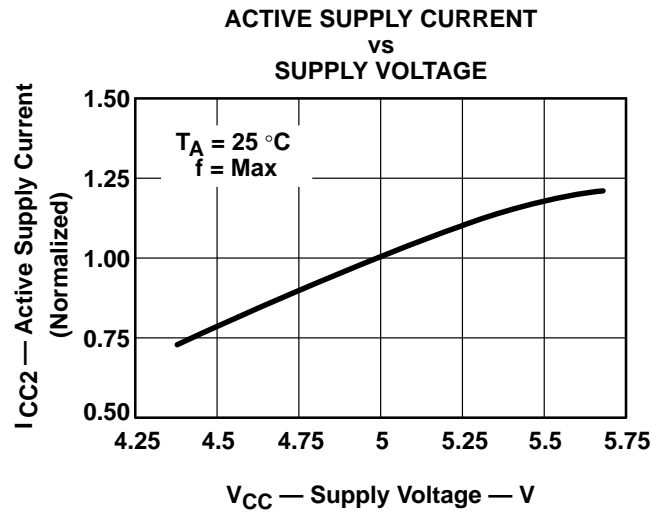
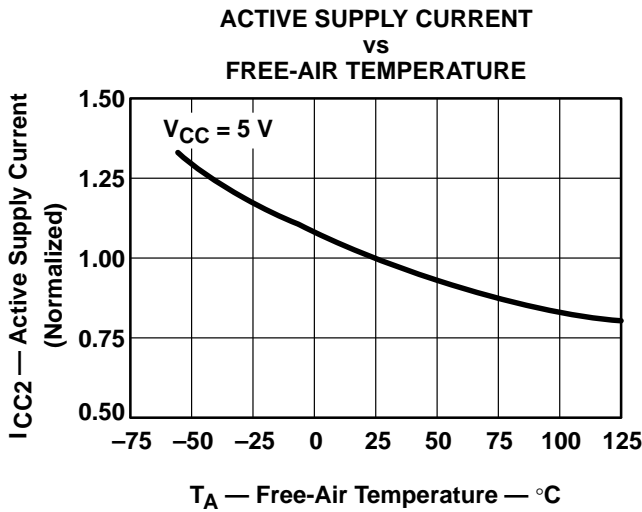
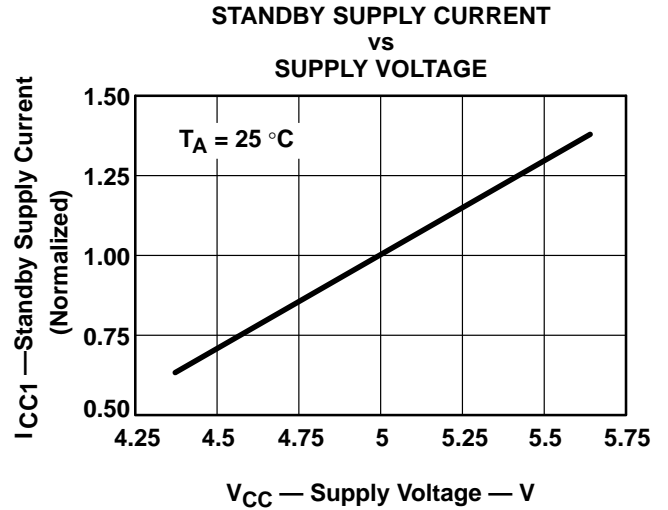
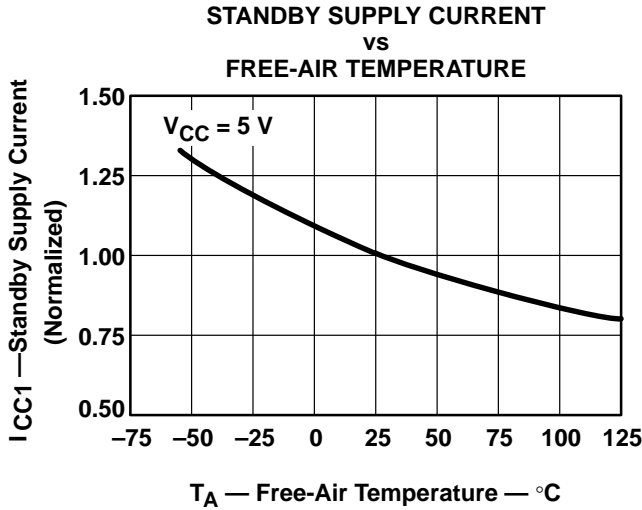
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device symbolization

This data sheet is applicable to all TI TMS27C128 CMOS EPROMs and TMS27PC128 PROMs with the data sheet revision code "B" as shown below.



TYPICAL TMS27C/PC128 CHARACTERISTICS



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